AMENDMENTS TO THE CLAIMS

1.   (Original) A memory including at least one row, the at least one row comprising:

a first row segment having a first plurality of memory cells coupled to a first dataline segment;

a second row segment having a second plurality of memory cells coupled to second dataline segment; and

a dataline driver connected between the first and second dataline segments and having inputs to receive read and write control signals, the dataline driver configurable to propagate data only in a first direction from the second row segment to the first row segment during a read operation and to propagate data only in a second direction from the first row segment to the second row segment during a write operation.

2.   (Original) The memory of Claim 1, wherein the dataline driver includes outputs to provide the read and write control signals to a dataline driver in a second row of the memory.

3.   (Original) The memory of Claim 1, wherein the dataline driver is configurable to selectively drive the first dataline segment in response to the second dataline segment during read operations and to selectively drive the second dataline segment in response to the first dataline segment during write operations.

4.   (Original) The memory of Claim 1, wherein the first dataline segment is not connected to the second dataline segment.

5.   (Original) The memory of Claim 1, wherein the dataline driver comprises:

a first pull-up transistor coupled between a supply voltage and the second dataline segment;

a first pull-down transistor coupled between the second dataline segment and ground potential;

a first NAND gate having a first input coupled to the first dataline segment, a second input responsive to the write control signal, and an output coupled to a gate of the first pull-up transistor; and

a first NOR gate having a first input coupled to the first dataline segment, a second input responsive to the write control signal, and an output coupled to a gate of the first pull-down transistor.

6.   (Original) The memory of Claim 5, wherein the dataline driver further comprises:

a second pull-down transistor coupled between the first dataline segment and ground potential; and

a second NOR gate having a first input coupled to the second dataline segment, a second input responsive to the read control signal, and an output coupled to a gate of the second pull-down transistor.

7.   (Original) The memory of Claim 6, wherein the dataline driver further comprises:

a second pull-up transistor coupled between the supply voltage and the first dataline segment; and

a second NAND gate having a first input coupled to the second dataline segment, a second input responsive to the read control signal, and an output coupled to a gate of the second pull-up transistor.

8.   (Original) The memory of Claim 1, wherein the first row segment includes a keeper latch, comprising:

a strong inverter having an input coupled to the first dataline segment and having an output; and

a weak inverter having an input coupled to the output of the strong inverter and having an output coupled to the first dataline segment.

9.   (Original) The memory of Claim 1, wherein the first row segment and the dataline driver comprise a tile adapted to be replicated any number of times to form the at least one row.

10.   (Original) The memory of Claim 9, wherein the tile further comprises the second row segment.

11.   (Original) The memory of Claim 1, wherein the first and second row segments have an equal number of memory cells.

12.   (Original) The memory of Claim 1, further comprising a control circuit coupled to the first dataline segment, the control circuit configurable to pre-discharge the first dataline segment.

13.   (Original) The memory of Claim 12, wherein the dataline driver is configurable to pre-discharge the second dataline segment.

14.   (Original) The memory of Claim 12, wherein the control circuit further comprises:
    a logic circuit having first inputs to receive one or more control signals, a second input to receive write data, and first and second outputs;
    a pull-up transistor coupled between a supply voltage and the first dataline segment and having a gate coupled to the first output of the logic circuit; and
    a pull-down transistor coupled between the first dataline segment and ground potential and having a gate coupled to the second output of the logic circuit.

15.   (Original) The memory of Claim 14, wherein the logic circuit is configurable to tri-state the first dataline segment in response to the control signals.

16.   (Original) The memory of Claim 14, wherein the logic circuit comprises:
    a first portion for generating first charge and discharge signals in response to

the write data being of a first logic state;

a second portion for generating second charge and discharge signals in response to the write data being of a second logic state; and

at least one third portion for selectively providing either the first charge and discharge signals or the second charge and discharge signals to the respective gates of the pull-up and pull-down transistors in a corresponding row.

17.   (Original) The memory of Claim 16, wherein the at least one third portion comprises a multiplexer circuit.

18.   (Original) The memory of Claim 16, wherein the first charge and discharge signals and the second charge and discharge signals are provided concurrently to each row in the memory.

19.   (Original) The memory of Claim 18, wherein the first and second portions of the logic circuit are not associated with any one row.

20.   (Original) The memory of Claim 18, wherein each row is associated with a corresponding third portion of the logic circuit.

21.   (Original) The memory of Claim 1, wherein the first and second dataline segments each comprise a pair of complementary dataline segments.

22.   (Original) The memory of Claim 21, wherein the memory cells comprise SRAM cells connected between the complementary dataline segments.

23.   (Original) The memory of Claim 1, wherein the memory is a configuration memory for a programmable logic device.

24.   (Original) The memory of Claim 1, wherein the dataline driver the dataline driver is further configurable to propagate data in the first and second

directions at a plurality of voltage levels.

25.   (Original) A memory including any number of rows, each row comprising:

a plurality of row segments, each having a plurality of memory cells coupled to a corresponding dataline segment; and

a plurality of dataline drivers, each connected to the dataline segments in first and second adjacent row segments and configured to drive the dataline segment in the first adjacent row segment in response to a logical combination of a control signal and data on the dataline segment in the second adjacent row segment.

26.   (Original) The memory of Claim 25, wherein the control signal comprises read and write signals.

27.   (Original) The memory of Claim 25, wherein the dataline driver is configured to propagate data only from the dataline segment in the first adjacent row segment to the dataline segment in the second adjacent row segment during write operations and configured to propagate data only from the dataline segment in the second adjacent row segment to the dataline segment in the first adjacent row segment during read operations.

28.   (Original) The memory of Claim 25, wherein each dataline driver comprises:

a first pull-up transistor coupled between a supply voltage and the dataline segment in the second adjacent row segment;

a first pull-down transistor coupled between the dataline segment in the second adjacent row segment and ground potential;

a first NAND gate having a first input coupled to the dataline segment in the first adjacent row segment, a second input responsive to the control signal, and an output coupled to a gate of the first pull-up transistor; and

a first NOR gate having a first input coupled to the dataline segment in the first

adjacent row segment, a second input responsive to the control signal, and an output coupled to a gate of the first pull-down transistor.

29.   (Original) The memory of Claim 28, wherein the dataline driver further comprises:

a second pull-down transistor coupled between the dataline segment in the first adjacent row segment and ground potential; and

a second NOR gate having a first input coupled to the dataline segment in the second adjacent row segment, a second input responsive to the control signal, and an output coupled to a gate of the second pull-down transistor.

30.   (Original) The memory of Claim 29, wherein the dataline driver further comprises:

a second pull-up transistor coupled between the supply voltage and the dataline segment in the first adjacent row segment; and

a second NAND gate having a first input coupled to the dataline segment in the second adjacent row segment, a second input responsive to the control signal, and an output coupled to a gate of the second pull-up transistor.

31.   (Original) The memory of Claim 25, wherein the dataline segments in the first and second adjacent row segments each comprise a pair of complementary dataline segments.

32.   (Original) The memory system of Claim 25, wherein each row segment further comprises a keeper latch having a drive strength configured to compensate for leakage currents in the corresponding row segment without disturbing read operations.

33.   (Original) The memory of Claim 25, wherein the memory comprises a configuration memory in a programmable logic device.

34.   (Original) A memory including any number of rows, each row comprising:

a plurality of row segments, each having a plurality of memory cells coupled to a corresponding dataline segment; and

a plurality of dataline drivers, each connected to the dataline segment in adjacent row segments and comprising:

a first pull-up transistor coupled between a supply voltage and the dataline segment in a first adjacent row segment;

a first pull-down transistor coupled between the dataline segment in the first adjacent row segment and ground potential;

a first NAND gate having a first input coupled to the dataline segment in a second adjacent row segment, a second input responsive to a control signal, and an output coupled to a gate of the first pull-up transistor; and

a first NOR gate having a first input coupled to the dataline segment in the second adjacent row segment, a second input responsive to the control signal, and an output coupled to a gate of the first pull-down transistor.

35.   (Original) The memory of Claim 34, wherein the dataline driver further comprises:

a second pull-down transistor coupled between the dataline segment in the second adjacent row segment and ground potential; and

a second NOR gate having a first input coupled to the dataline segment in the first adjacent row segment, a second input responsive to the control signal, and an output coupled to a gate of the second pull-down transistor.

36.   (Original) The memory of Claim 35, wherein the dataline driver further comprises:

a second pull-up transistor coupled between the supply voltage and the dataline segment in the second adjacent row segment; and

a second NAND gate having a first input coupled to the dataline segment in the first adjacent row segment, a second input responsive to the control signal, and an

output coupled to a gate of the second pull-up transistor.

37.   (Original) The memory of Claim 34, wherein the memory comprises a configuration memory for a programmable logic device.

38.   (Original) A method of operating a memory having a plurality of row segments each having a dataline segment connected to a dataline segment in an adjacent row segment by a corresponding dataline driver, comprising:

configuring each dataline driver to propagate data only in a first direction from a previous row segment to a next row segment during write operations; and

configuring each dataline driver to propagate data only in a second direction from the next row segment to the previous row segment during read operations.

39.   (Original) The method of Claim 38, further comprising:

for each row segment, providing a keeper latch to maintain the corresponding dataline segment in its current logic state; and

sizing the keeper latches to compensate for leakage currents in corresponding row segments without disturbing read operations.

40.   (Original) The method of Claim 38, further comprising:

selectively charging the dataline segment in the next row segment in response to a first logical combination of data on the dataline segment in the previous row segment and a control signal using a first pull-up transistor; and

selectively discharging the dataline segment in the next row segment in response to a second logical combination of data on the dataline segment in the previous row segment and the control signal using a first pull-down transistor.

41.   (Original) The method of Claim 40, further comprising:

selectively discharging the dataline segment in the previous row segment in response to a third logical combination of data on the dataline segment in the next row segment and the control signal using a second pull-down transistor.

42.   (Original) The method of Claim 41, further comprising:

selectively charging the dataline segment in the previous row segment in response to a fourth logical combination of data on the dataline segment in the next row segment and the control signal using a second pull-up transistor.

43.   (Withdrawn) A method of testing one or more transistors that form a latch having an output connected to a dataline and having a complementary output connected to a complementary dataline, comprising:

writing a first logic value to the latch;

pre-discharging the datalines to logic low states;

selecting the latch to stress a first PMOS pull-up transistor in the latch;

pre-charging the datalines to logic high states;

reading data from the latch; and

designating the first PMOS pull-up transistor as defective if the data read from the latch does not match the first logic value.

44.   (Withdrawn) The method of Claim 43, further comprising:

writing a second logic value to the latch;

pre-discharging the datalines to logic low states;

selecting the latch to stress a second PMOS pull-up transistor in the latch;

pre-charging the datalines to logic high states;

reading data from the latch; and

designating the second PMOS pull-up transistor as defective if the data read from the latch does not match the second logic value.

45.   (Withdrawn) The method of Claim 44, further comprising:

writing the first logic value to the latch;

pre-charging the datalines to logic high states;

reading data from the latch; and

designating a first NMOS pull-down transistor as defective if the data read from the latch does not match the first logic value.

46.   (Withdrawn) The method of Claim 45, further comprising:

writing the second logic value to the latch;

pre-charging the datalines to logic high states;

reading data from the latch; and

designating a second NMOS pull-down transistor as defective if the data read from the latch does not match the second logic value.

47.   (Withdrawn) The method of Claim 46, wherein the latch comprises an SRAM cell.